REMARKS

Claims 1, 3, 5-7 and 10 are pending in this application with claims 1 and 10 being amended and claim 4 being cancelled by this response. Claims 2, 8, 9 and 11 had been cancelled in a previous response. Claim 10 has been amended to indicate that the first graphics object and the second graphics object are mixed with a video stream. Claim 10 has also been amended as suggested by the Examiner in the Response to Argument section of the Office Action to clarify that the mixing is performed in an entity separate from the OSD processor and removing the repetitions. Claim 1 has been amended similarly. Support for the amendments to claims 1 and 10 may be found throughout the originally filed specification and drawing figures and more specifically on page 5, lines 18-21 and page 6, lines 12-31. Thus, it is respectfully submitted that no new matter is added by the amendments to the claims.

Rejection of claims 1, 3-7 and 10 under 35 U.S.C. 103(a)

Claims 1, 3-7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Valmiki et al. (U.S. Patent No. 6,636,222) in view of Terao et al. (U.S. Publication No. 2001/0055011) and further in view of Li et al. (U.S. Publication No. 2003/0043172) and Miyamoto (U.S. Patent No. 6,839,071).

The failure of an asserted combination to teach or suggest each and every feature of a claim remains fatal to an obviousness rejection under 35 U.S.C. § 103. Section 2143.03 of the MPEP requires the "consideration" of every claim feature in an obviousness determination. To render a claim unpatentable, however, the Office must do more than merely "consider" each and every feature for this claim. Instead, the asserted combination of the patents must also teach or suggest *each and every claim feature. See In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974) (emphasis added) (to establish *prima facie* obviousness of a claimed invention, all the claim features must be taught or suggested by the prior art). Indeed, as the Board of Patent Appeals and Interferences has confirmed, a proper obviousness determination requires that an Examiner make "a searching comparison of the claimed invention - *including all its*

limitations - with the teaching of the prior art." *See In re Wada and Murphy*, Appeal 2007-3733, *citing In re Ochiai*, 71 F.3d 1565, 1572 (Fed. Cir. 1995) (emphasis in original). "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious" (MPEP §2143.03, citing *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)).

The present claimed arrangement provides an electronic apparatus and process for generating a video signal. A command to display a first and a second graphics object is received. A possible overlap between the first and the second graphics object is detected. If there is an absence of overlap, an OSD processor generates a digital stream representing the first graphics object and the second graphics object and generates a video signal based on a mixing of the digital stream with a video stream received from a memory. The OSD processor is unable to manage two graphics objects that overlap. If there is a presence of overlap, the OSD processor generates a first digital stream representing a first graphics object. The second graphics object is converted into a still picture and the still picture is written to memory. A second digital stream is generated from the still picture in the memory. The first digital stream received from the OSD processor, the second digital stream generated from the still picture received from the memory, and a video stream are mixed. A video signal is generated from the mixture.

The present claimed arrangement advantageously allows the display of the two overlapping graphics, despite the inability of the OSD processor to perform such display on its own by converting the second of the two overlapped graphics into a stationary picture in a memory separate from the OSD path, which in turn is combined by a mixer with the OSD plane containing the first graphic. For the reasons presented below, Applicant respectfully submits that Valmiki, Terao, Li and Miyamoto fail to teach or suggest each feature of the present claimed arrangement.

Valmiki describes a video and graphics system which processes video data including both analog video, e.g., NTSC/PAL/SECAM/S-video, and digital video, e.g., MPEG-2 video in SDTV or HDTV format. The video and graphics system includes a video decoder, which is capable of concurrently decoding multiple SLICEs of MPEG-2 video data. The video decoder includes multiple row decoding engines for decoding the MPEG-2 video data. Each row decoding engine concurrently decodes two or more rows of the MPEG-2 video data. The row decoding engines have a pipelined architecture for concurrently decoding multiple rows of MPEG-2 video data. The video decoder may be integrated on an integrated circuit chip with other video and graphics system components such as transport processors for receiving one or more compressed data streams and for extracting video data, and a video compositor for blending processed video data with graphics (see Abstract). However, Valmiki is not concerned with working around the limitations of OSD processors, but instead with rendering compressed video data within an allotted number of clock cycles.

Terao describes an invention whose goal is to provide an information processor which, in case a component in which a moving picture is displayed is overlapped by another window, can apply display effect only to a region on which the moving picture is actually displayed (see Abstract). Terao is concerned with improving an image on a CRT display, but only applies the improvement to the region of the moving picture that is displayed (see paragraphs [0002]-[0004] and [0007]-[0008]). However, Terao does not teach or suggest means for converting one of the graphics object into picture data if the overlap cue is generated.

Li describes a method for extracting textual and graphical overlays from video sequences involving steps of detecting a potential overlay in a video sequence and then verifying that the potential overlay is an actual overlay. Detection of textual overlays involves wavelet decomposition and neural network processing, while detection of graphical overlays involves template matching. Verification of textual and graphical overlays involves spatial and/or temporal verification (see Abstract). Li is directed at

receiving a video signal with a previously applied textual overlay and reversing the overlay process whereas the present claimed arrangement is directed at creating a composite OSD for mixture with a video signal. Li operates on a single graphics object, a video frame, to create multiple graphics objects.

Page 6 of the Office Action concedes that the combination of Valkimi, Terao and Li, similar to the individual systems, fails to teach or suggest mixing means for mixing said first digital stream and said second graphics object into a video signal. Therefore, these references when taken alone or in any combination cannot teach or suggest "mixing means for mixing said first digital stream, received from said OSD processor, said second digital stream, received from said still picture data, and of a video stream received from the video memory, into a video signal" as recited in amended claim 1 of the present arrangement. However, the Office Action cites Miyamoto as teaching the aforementioned feature. Applicant respectfully disagrees.

Miyamoto describes an apparatus and method for receiving a first display information from a first device and a second display information and control information from a second device. A display unit displays the first display information and the second display information on a display unit. A control until generates control information for minimizing overlay of the first display information and the second information. Control information is received from the control unit and sent to the second device before receiving the second display information (see Abstract).

However, Miyamoto, similar to Valkimi, Terao and Li, fails to teach or suggest "mixing means for mixing said first digital stream, received from said OSD processor, said second digital stream, received from said still picture data, and of a video stream received from the video memory, into a video signal" as recited in amended claim 1 of the present arrangement. Miyamoto deals with home networks including Audio-Video apparatuses. Miyamoto is concerned with the problem of receiving OSDs from a plurality of apparatuses irrespective of layout on the display picture surface of the

display device. Miyamoto describes a method for setting drawing conditions (see column 11, line 56 – column 14, line 47 and figure 7). Miyamoto describes the detection of overlapped portions and on presence of overlapped portions, overlay conditions of the OSDs are checked. OSDs may then be overlaid or not, with or without the still image being changed. Unlike the present claimed arrangement, Miyamoto does not describe mixing the first digital stream received from the OSD processor, the second digital stream received from the still picture data, and of a video stream received from the video memory, into a video signal. In addition, Miyamoto is silent regarding how the OSDs are transmitted to the display. Therefore, Miyamoto, similar to Valkimi, Terao and Li, does not teach or suggest "mixing means for mixing said first digital stream, received from said OSD processor, said second digital stream, received from said still picture data, and of a video stream received from the video memory, into a video signal" as recited in amended claim 1 of the present arrangement.

In addition, the combination of Valmiki, Terao, Li and Miyamoto, similar to the individual systems, neither teaches nor suggests the features of the present claimed arrangement. Specifically, the combination of Valmiki, Terao, Li, Huang and Miyamoto, as discussed above, neither teaches nor suggests "mixing means for mixing said first digital stream, received from said OSD processor, said second digital stream, received from said still picture data, and of a video stream received from the video memory, into a video signal" as recited in amended claim 1 of the present arrangement. Therefore, it is respectfully submitted that the rejection of claim 1 is overcome and should be withdrawn.

Claims 3 and 5-7 are dependent on claim 1 and are considered patentable for the reasons presented above with respect to claim 1. Claim 10 includes similar features to claim 1 discussed above and is considered patentable for the reasons presented above with respect to claim 1.

In view of the above remarks and amendments to claims 1 and 10, it is respectfully submitted that the present claimed arrangement is not unpatentable over Valmiki, Terao, Li and Miyamoto. Therefore, it is respectfully submitted that this rejection has been overcome and should be withdrawn.

Rejection of claims 1, 3-7 and 10 under 35 U.S.C. 103(a)

Claims 1, 3-7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Valmiki et al. (U.S. Patent No. 6,636,222) in view of Terao et al. (U.S. Publication No. 2001/0055011) and further in view of Li et al. (U.S. Publication No. 2003/0043172), Huang et al. (U.S. Publication No. 2003/0169371) and Miyamoto (U.S. Patent No. 6,839,071).

As the body of the rejection is only directed toward claim 10, Applicant believes the rejection of claims 1 and 3-7 was inadvertently included in the heading. However, for completeness, Applicant will respond to the rejection as if claims 1 and 3-7 were meant to be included.

The present claimed arrangement provides an electronic apparatus and process for generating a video signal. A command to display a first and a second graphics object is received. A possible overlap between the first and the second graphics object is detected. If there is an absence of overlap, an OSD processor generates a digital stream representing the first graphics object and the second graphics object and generates a video signal based on a mixing of the digital stream with a video stream received from a memory. The OSD processor is unable to manage two graphics objects that overlap. If there is a presence of overlap, the OSD processor generates a first digital stream representing a first graphics object. The second graphics object is converted into a still picture and the still picture is written to memory. A second digital stream is generated from the still picture in the memory. The first digital stream

received from the OSD processor, the second digital stream generated from the still picture received from the memory, and a video stream are mixed. A video signal is generated from the mixture.

The present claimed arrangement advantageously allows the display of the two overlapping graphics, despite the inability of the OSD processor to perform such display on its own by converting the second of the two overlapped graphics into a stationary picture in a memory separate from the OSD path, which in turn is combined by a mixer with the OSD plane containing the first graphic. For the reasons presented below, Applicant respectfully submits that Valmiki, Terao, Li, Huang and Miyamoto, taken alone or in any combination, fail to teach or suggest each feature of the present claimed arrangement.

Valmiki describes a video and graphics system which processes video data including both analog video, e.g., NTSC/PAL/SECAM/S-video, and digital video, e.g., MPEG-2 video in SDTV or HDTV format. The video and graphics system includes a video decoder, which is capable of concurrently decoding multiple SLICEs of MPEG-2 video data. The video decoder includes multiple row decoding engines for decoding the MPEG-2 video data. Each row decoding engine concurrently decodes two or more rows of the MPEG-2 video data. The row decoding engines have a pipelined architecture for concurrently decoding multiple rows of MPEG-2 video data. The video decoder may be integrated on an integrated circuit chip with other video and graphics system components such as transport processors for receiving one or more compressed data streams and for extracting video data, and a video compositor for blending processed video data with graphics (see Abstract). However, Valmiki is not concerned with working around the limitations of OSD processors, but instead with rendering compressed video data within an allotted number of clock cycles.

Terao describes an invention whose goal is to provide an information processor which, in case a component in which a moving picture is displayed is overlapped by

another window, can apply display effect only to a region on which the moving picture is actually displayed (see Abstract). Terao is concerned with improving an image on a CRT display, but only applies the improvement to the region of the moving picture that is displayed (see paragraphs [0002]-[0004] and [0007]-[0008]). However, Terao does not teach or suggest means for converting one of the graphics object into picture data if the overlap cue is generated.

Li describes a method for extracting textual and graphical overlays from video sequences involving steps of detecting a potential overlay in a video sequence and then verifying that the potential overlay is an actual overlay. Detection of textual overlays involves wavelet decomposition and neural network processing, while detection of graphical overlays involves template matching. Verification of textual and graphical overlays involves spatial and/or temporal verification (see Abstract). Li is directed at receiving a video signal with a previously applied textual overlay and reversing the overlay process whereas the present claimed arrangement are directed at creating a composite OSD for mixture with a video signal. Li operates on a single graphics object, a video frame, to create multiple graphics objects.

Page 10 of the Office Action concedes that the combination of Valkimi, Terao and Li, similar to the individual systems, does not teach or suggest that the OSD processor is unable to manage the graphics objects that overlap and therefore, cannot teach or suggest the steps claimed in the present arrangement in the presence of an overlap. However, the Office Action cites Huang as teaching where the OSD processor may be set such that the OSD processor is disabled from processing video overlaying and concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the teachings of Valmiki, Terao and Li to incorporate wherein said OSD processor is unable to manage two graphics objects that overlap for the benefit of decreasing fabrication costs and utilizing current hardware capability to manage the OSD content within system memory or local memory for flexibility. Applicant respectfully disagrees.

Huang describes a method for controlling various modes of OSD functions in a display system. The method uses a display buffer with plural register for storing frame data, which corresponds to a frame. A memory is used for storing OSD data, corresponding to an OSD window included in the frame. The micro-controller copies the OSD data in the register which corresponds to the OSD window by a data processing method (see Abstract).

However, Huang, similar to Valkimi, Terao and Li, fails to teach or suggest that in "presence of an overlap: generation by said OSD processor of a first digital stream representing a first graphics object; conversion of the second graphics object into a still picture; writing of the still picture to a memory; generation of a second digital stream from said still picture in the memory; mixing of the first digital stream, received from said OSD processor, of the second digital stream, generated from said still picture received from said memory and of a video stream; and generation of a video signal from said mixture" as recited in amended claim 10 of the present arrangement. Huang is directed at the problem that conventional OSD circuits lack flexibility in providing multiple windows simultaneously. Unlike the present claimed arrangement, Huang is silent in regards to converting one of two overlapping graphics objects into picture data for subsequent mixing with an OSD stream. Therefore, Huang also fails to address the problem of an OSD processor which is unable to manage two graphics objects that overlap and thus fails to teach or suggest the steps claimed in amended claim 10 of the present arrangement in the presence of an overlap.

Additionally, page 11 of the Office Action concedes that the combination of Valkimi, Terao, Li and Huang, similar to the individual systems, does not teach or suggest mixing means for mixing said first digital stream and said second graphics object into a video signal. Therefore, these references when taken alone or in any combination cannot teach or suggest "mixing of the first digital stream, received from said OSD processor, of the second digital stream, generated from said still picture

received from said memory and of a video stream" as recited in amended claim 10 of the present arrangement. However, the Office Action cites Miyamoto as teaching the aforementioned feature. Applicant respectfully disagrees.

Miyamoto describes an apparatus and method for receiving a first display information from a first device and a second display information and control information from a second device. A display unit displays the first display information and the second display information on a display unit. A control until generates control information for minimizing overlay of the first display information and the second information. Control information is received from the control unit and sent to the second device before receiving the second display information (see Abstract).

However, Miyamoto, similar to Valkimi, Terao, Li and Huang, fails to teach or suggest "mixing of the first digital stream, received from said OSD processor, of the second digital stream, generated from said still picture received from said memory and of a video stream" to generate a video signal as recited in amended claim 10 of the present arrangement. Miyamoto deals with home networks including Audio-Video apparatuses. Miyamoto is concerned with the problem of receiving OSDs from a plurality of apparatuses irrespective of layout on the display picture surface of the display device. Miyamoto describes a method for setting drawing conditions (see column 11, line 56 – column 14, line 47 and figure 7). Miyamoto describes the detection of overlapped portions and on presence of overlapped portions, overlay conditions of the OSDs are checked. OSDs may then be overlaid or not, with or without the still image being changed. Unlike the present claimed arrangement, Miyamoto does not describe mixing the first digital stream received from the OSD processor, the second digital stream received from the still picture data, and of a video stream received from the video memory, into a video signal. In addition, Miyamoto is silent regarding how the OSDs are transmitted to the display. Therefore, Miyamoto, similar to Valkimi, Terao, Li and Huang, does not teach or suggest "mixing of the first digital stream, received from said OSD processor, of the second digital stream,

generated from said still picture received from said memory and of a video stream" to generate a video signal as recited in amended claim 10 of the present arrangement.

In addition, the combination of Valmiki, Terao, Li, Huang and Miyamoto, similar to the individual systems, neither teaches nor suggests the features of the present claimed arrangement. Specifically, the combination of Valmiki, Terao, Li, Huang and Miyamoto, as discussed above, neither teaches nor suggests "mixing of the first digital stream, received from said OSD processor, of the second digital stream, generated from said still picture received from said memory and of a video stream" to generate a video signal as recited in amended claim 10 of the present arrangement. In addition, the combination of Valmiki, Terao, Li, Huang and Miyamoto, similar to the individual systems, also fails to address the problem of an OSD processor which is unable to manage two graphic objects that overlap as recited in the present claimed arrangement. Thus, the combination of Valmiki, Terao, Li, Huang and Miyamoto, similar to the individual systems, neither teaches nor suggests each feature of amended claim 10 of the present arrangement. Therefore, it is respectfully submitted that the rejection of claim 10 is overcome and should be withdrawn.

Claim 1 includes similar features to claim 10 discussed above and is considered patentable for the reasons presented above with respect to claim 10. Claims 3 and 5-7 are dependent on claim 1 and are considered patentable for the reasons presented above with respect to claim 1.

Claim 4 has been cancelled by this response. Claims 2, 8, 9 and 11 had been cancelled in a previous response.

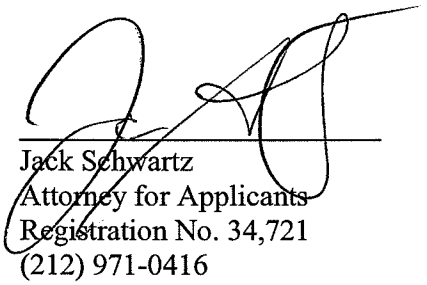
In view of the above remarks and amendments to claims 1 and 10, it is respectfully submitted that the present claimed arrangement is not unpatentable over Valmiki, Terao, Li, Huang and Miyamoto. Therefore, it is respectfully submitted that this rejection has been overcome and should be withdrawn.

Having fully addressed the Examiner's rejections, it is believed that, in view of the amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at the phone number below, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due. However, if a fee is due, please charge the fee to Deposit Account 07-0832.

Respectfully submitted,
Edouard Ritz

Date: September 9, 2011



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